REMARKS/ARGUMENTS

Favorable reconsideration of this application as presently amended and in light of the following remarks is respectfully requested.

Claims 1-23 and 27-29 are presently active in this application, Claims 1, 6-8, 13-15, 21-23 and 29 having been amended by the present Amendment.

In the outstanding Office Action Claims 1-23 and 27-29 were rejected under 35 USC §102(e) as being anticipated by Thekkath et al (U.S. Patent 6,604,159, hereinafter "Thekkath").

By way of this amendment and reply to the Office Action mailed September 22, 2005, Claims 1, 6-8, 13-15, 21-23 and 29 have been amended. Support for the amendments to independent claims 1, 8, 15, 21 - 23 and 29 may be found on page 8, lines 14 to page 9, line 26 of the specification and Figs. 5 and 6 of the drawings. Therefore, no new matter has been added.

Applicants respectfully traverse the rejection of Claims 1-23 and 27-29 under 35 U.S.C. 102(e), as being anticipated by Thekkath, because in Applicants' view, the claimed invention is clearly patentably distinguishing over the cited art.

Claim 1 recites, in part,

> the bus request signal is sent to said bus controller prior to data transfer and has a field comprising a plurality of bits for specifying necessary bit width, each of said plurality of bits identifying a respective one of said unit data buses, and said bus controller grants the use of each of said unit data buses specified by the bits of said bus request signal.

Claims 8, 15, 21-23 and 29 recite similar features.

Thekkath describes an on-chip split transaction system bus which includes a data bus request signal which is sent to a bus arbiter.

In the outstanding Official Action, Thekkath is cited as disclosing every limitation of the claims of the present invention.

However, Thekkath does not describe or suggest that the bus request signal is sent to said bus controller prior to data transfer and has a field comprising a plurality of bits for specifying necessary bit width, each of said plurality of bits identifying a respective one of said unit data buses.

In other words, in Thekkath the "data bus request signal" which is sent to the bus arbiter,[1] does not contain information capable of identifying any of the "data lines" of the system bus 610 of Fig. 6, or any of the "data ID lines" of system bus 410 of Fig. 4. As is apparent from Figures 6 and 8b, the "data bus request signal" of Thekkath is described as an "MDA_req" signal 652, however this signal lacks any operand for identifying any of the "data lines." In contrast, the present claims describes a bus request signal which has a field comprising a plurality of bits, each of the plurality of bits identifying a respective one of said unit data buses.

Additionally, the outstanding Office Action states on Page 3 that the transaction ID of Thekkath is associated with a request which corresponds to each data line. However, the "request" signal of Thekkath described in Col. 8 is sent from the request master to another master to solicit a data response during the data transfer. In contrast, the claimed bus request signal is sent to the bus controller prior to data transfer. Thus, the "request" signal of Thekkath described above does not describe the bus request signal described in Claim 1 and similarly in independent Claims 8, 15, 21-23 and 29.

Further, the "transaction ID" which is specified along with "request" in Thekkath is generated by concatenating the current requester's (bus master) id with the index of the transaction buffer entry that will hold the request until a response is returned.[2] Since in Thekkath the transaction buffer entry is used for allowing out-of-order returns of the "response" with the data in response to the "request", each entry of the transaction buffer

[1] Thekkath, col. 4, lines 13-15.
[2] Thekkath, col. 8, lines 60-65.

does not correspond to "each of unit data buses" described in the independent claims. Instead each entry of the transaction buffer corresponds to a "request" which might be serially sent from one bus master (requester) asynchronous of the "response".

Additionally, the outstanding Office Action states at the end of page 2 that "data bus comprises data lines each data line correspond to particular bus master." However, in Fig. 6, 610 and col. 5, lines 25-36, Thekkath does not describe or suggest that each data line corresponds to a particular bus master, instead Thekkath merely descrives that a plurality of bus masters 601, 602 are connected to bus 610 and the bus may comprise "data lines".

Therefore, Thekkath fails to disclose all of the features of the present invention described in the claims. For example, Thekkath fails to describe or suggest the claimed "plurality of bus masters connected to each of the unit data buses and configured to send a bus request signal requesting to acquire a use of each of said unit data buses... the bus request signal is sent to said bus controller prior to data transfer and has a field comprising a plurality of bits for specifying necessary bit width, each of said plurality of bits identifying a respective one of said unit data buses, and said bus controller grants the use of each of said unit data buses specified by the bits of said bus request signal."

Thus, Applicants respectfully submit that independent Claims 1, 8, 15, 21-23 and 29 and claims depending therefrom, patentably distinguish over Thekkath.

Consequently, in light of the above discussion and in view of the present amendment, the present application is believed to be in condition for allowance and an early and favorable action to that effect is respectfully requested.

Respectfully submitted,

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